Dr. PRATEEK AGARWAL Phone: +91-7599222718 Email: prateek.aggrawal@gkv.ac.in

Career Objective: To gain a challenging position in the field of Academics by acquiring requisite skills and maximizing my capabilities while contributing to the growth of the organization that I work for.

Academic Profile:

- Ph.D. (2025) Electronics Engineering from **Faculty of Engg. & Tech., Gurukula Kangri (Deemed to be University)**, Haridwar, Uttarakhand.
- M.Tech. (2008) Electronics & Communication from **Thapar University** (TU), Patiala, Punjab.
- B.Tech. (2006) Electronics & Communication from U.P.Technical University, Lucknow, U.P.

Career Profile: **15 Years** Experiences **[**Research & Academics: 15 Years**]**

- October 2010 – Continue: Asst. Professor, Dept of Electronics & Comm. Engg. **Faculty of Engg. & Tech., Gurukula Kangri (Deemed to be University)**, Haridwar. Uttarakhand

Achievements:	**Subjects & Skills:**	**Exam Qualified:**
• 379-score in GATE-2005	• Electronic Devices	GATE
• 481-score in GATE-2010	• VLSI Technology	
• **04 SCI/SCIE** Research Articles	• VLSI Design	
	• Analog Circuits	
	• Digital Electronics	

Research Area:FPGA, NoC, Router.

Soft-Skills: Xilinx ISE 14.7, Modelsim 10.0.

Research Publications: **12** [**SCI-4**, SCOPUS-1, Book Chapter-1, Conference-6]

Patents Published: 01 [Indian IPR-01]

Research Work at Faculty of Engg. & Tech., Gurukula Kangri (Deemed to be University), Haridwar during PHD Program:

The thesis **"Design and Implementation of Low Power Digital Circuit for Nano Computing Applications"** presents a thoughtful and timely contribution to the field of low-power VLSI circuit design, especially for applications where energy efficiency, compactness, and performance are critical. In an era where portable devices and high-speed communication systems dominate the landscape, the development of FPGA-based router chips that support scalable, parallel and secure data communication is both relevant and impactful. The work not only explores 2D and 3D Network-on-Chip (NoC) architectures across various FPGA platforms but also integrates RSA encryption to ensure secure transmission—an essential feature for modern sensory and wireless networks. The clear focus on reducing power consumption without compromising performance makes this project highly suitable for

next-generation embedded and high-performance computing systems. Given the thorough design process, successful simulation results and practical implementation insights, it is strongly recommended that this work be extended and applied in real-world systems. Further research and development in this direction can help meet the growing demand for efficient, scalable, and secure hardware solutions in the age of nano-scale electronics and IoT.

Responsibility @ Organization: **(1)** Time-Table Co-ordinator
(2) Member of accommodation committee of National and International Conferences

Research Publication in SCI/SCIE Journals [04]

- **Prateek Agrawal**, Tanuj Kumar Garg, Adesh Kumar "Analysis of 3D NoC router chip on different FPGA for minimum hardware and fast switching",*National Academy Science Letters*,vol.47,no.1,2024,pp.35-39.DOI: https://doi.org/10.1007/s40009-023-01295-y **[SCIE,IF-1.2]**
- **Prateek Agrawal**, Tanuj Kumar Garg, Adesh Kumar "Electronics Hardware Chip Design for Router–Router Communication",*Proc. Natl. Acad. Sci., India,Sect. A Phys. Sci.,*vol.93,no.4,2023,pp.703-710.DOI: https://doi.org/10.1007/s40010-023-00853-9 **[SCIE,IF-0.8]**
- **Prateek Agrawal**, Tanuj Kumar Garg, Adesh Kumar "Router Chip with RSA Embedded Security for Delay and Power Study in Sensory Data Communication", *Proc. Natl. Acad. Sci., India, Sect. A Phys. Sci.,India Section A: Physical Sciences,* vol.95, no.2, 2025, pp. 163-175. DOI: https://doi.org/10.1007/s40010-025-00916-z **[SCIE,IF-0.8]**
- Raghvendra Singh,Rajendra Singh,Rajendra Kumar Tripathi,**Prateek Agarwal** "Fingerprint Recognition using Artificial Neural Networks", *Proc. Natl. Acad. Sci., India, Sect. A Phys. Sci.,India Section A: Physical Sciences,* vol.95, no.2, 2025, pp. 127-135. DOI: https://doi.org/10.1007/s40010-025-00917-y **[SCIE,IF-0.8]**

Book Chapters Published in Proceedings [1]

- **Prateek Agrawal**, Tanuj Kumar Garg, Adesh Kumar "Low-power embedded system design applications using FPGAs", Embedded Devices & Internet of Things,CRC Press,Taylor & Francis Group,2024,pp 1-20. DOI: 10.1201/9781003510420 **[Scopus]**

Research Publications in SCOPUS [1]

- **Prateek Agarwal**, Tanuj Kumar Garg, Adesh Kumar "2D router chip design, analysis, and simulation for effective communication",*Int J Inf & Commun Technol*, vol. 12,no. 3,2023,pp 225-235,doi: 10.11591/ijict.v12i3.pp225-235. **[SCOPUS]**

Research Papers Accepted/Published/Presented in Conferences [6]

- **Prateek Agarwal**,Tanuj Kumar Garg,Adesh Kumar "Need of Low Power Simulators for Electronic Communication Systems", International Conference on Intelligent Communication, Control and

Devices(ICICCD-2024) at Electrical Cluster,School of Advanced Enginnering,UPES,Bidholi Campus,Dehradun,30-31 May, 2024.

- **Prateek Agarwal**,Tanuj Kumar Garg,Adesh Kumar "Low Power Estimation for Multibit Memory Writing and Reading in Hardware Chip Design", International Conference on Smart Devices (ICSD)at Uttaranchal University,Dehradun,02-03 May, 2024.DOI:10.1109/ICSD60021.2024.10751135
- **Prateek Agarwal**,Tanuj Kumar Garg,Adesh Kumar "Design of 64-Bit Vedic Logic Adder and Multiplier for Low Power and Fast Switching", International Conference on Veda Vijnana & Sanskriti Mahakumbha Gurukula Kangri(Deemed to be University) Haridwar, 23-25 December,2023.
- **Prateek Agarwal**,Tanuj Kumar Garg,Adesh Kumar "Router-Router Switching Communication and Logic Verification with Configured Hardware Chip", International Conference on Computer, Electronics and Electrical Engineering and their Applications(IC2E3-2023)at National Institute of Technology,Uttarakhand,08-09 June, 2023.DOI:10.1109/IC2E357697.2023.10262680
- Shivom, Harimohan Gaur,**Prateek Agarwal** "VLSI Empowered 4G Wireless Communications: A Review", National Conference Progress in Electronics & Allied Sciences(PEAS-2012) at Faculty of Engg. & Tech., Gurukul Kangri Vishwavidyalaya, Haridwar, 3-4 November, 2012.
- **Prateek Agarwal**, Parminder Singh Reel "Video Coding Standards and their Applications in Video Communication", National Conference ADVICE 2008 at NITTTR, Chandigarh, March, 2024.

Patent Publish/Grant [1]

Title: Method for Physical Intelligent VLSI Chip Design and Develop Technology

Application No.: 202111014696 form IP **India**

Event Organized/Coordinated at Institutions [1]

- Two Days Workshop/Hand-on Training on "VLSI Design & Chip Manufacturing" from 16th Nov to 17th Nov 2023 at Faculty of Engg. & Tech., Gurukula Kangri (Deemed to be University), Haridwar.

Name of Journals/Conferences, Associated as a Reviewer [5]

- National Academy Science Letters-India, Springer India.
- Proceedings of the National Academy Sciences Section A: Physical Sciences, NATL ACAD SCIENCES INDIA.
- Journal of Supercomputing, Springer.
- Energy Storage, Wiley.
- IEEE International Conferences.

Workshops/FDPs/STCs/ Presentations/Trainings/Seminars/Webinars Attended [15]

- National Webinar on "Quantum Information Processing" organized by Department of Electronics & Communication Engineering, INDUS University Ahemdabad,Gujrat on 3rd January 2022.
- AICTE Training And Learning(ATAL) Academy Online Elementary FDP on "Emergence of Reversible and Quantum Logic Circuits "from 22 November,2021 to 26 November,2021 at ABES Institute of Technology, Ghaziabad.
- Two week online Faculty Development Programme on "Recent trends in communication, networking and computing paradigms" organized by Department of Electronics & Communication Engineering, University College of Engineering & Technology, Bikaner Technical University, Bikaner from 7th to 18th September 2020 under TEQIP-III.
- Workshop on "Patents (Requirement, Filing, Strategy)"jointly organized by IPR Cell, Faculty of Engg. & Tech., Intellectual Property Rights Cell and External Affairs Interface Cell, Gurukula Kangri Vishwavidyalaya, Haridwar on 10 February, 2020.
- One week AICTE sponsored FDP on "Advanced Industrial Automation Technologies "from 08 July, 2019 to 13 July, 2019 organized by Uttarakhand Technical University, Dehradun under the aegis of TEQIP-III in collaboration with College of Engg. Roorkee, Roorkee.
- One week AICTE recognized STC on "Selection on Camera Shots and Editing for Video" from January 07, 2019 to January 11, 2019 organized by Educational Television Centre, NITTTR Chandigarh.
- FDP on "Teaching and Soft Skills" from 3 October,2018 to 4 October,2018 organized by Faculty of Engineering & Technology, Gurukula Kangri Vishwavidyalaya,Haridwar.
- TEQIP III sponsored one week STC on "Digital Signal and Image Processing" from June 22,2018 to June 26,2018 organized by Department of Computer Science and Engineering, GBPIET,Pauri-Garhwal,Uttarakhand.
- One week AICTE recognized STC on "MATLAB Based Design Simulation" from 07 March, 2016 to 11 March, 2016 organized by Department of Electronics and Communication Engineering, NITTTR Chandigarh.
- One week FDP on "Image Processing using VLSI Architectures" from 06 July, 2015 to 10 July, 2015 organized by Department of Electronics and Communication Engineering, IIT Roorkee.
- Workshop and Hands on Training on "Synthesis and Characterization of Thin Films" from 31st March to 1st April,2015 organized by Department of Physics, Gurukula Kangri Vishwavidyalaya, Haridwar.
- One week FDP on "Mobile Computing and Communication (MCC-2014)" from June 30,2014 to July 4,2014 organized by Department of Electronics and Communication Engineering, NIT Delhi.
- TEQIP II sponsored two weeks FDP/STTP on "ICT for Computing & Signal Processing" from 3 June, 2013 to 14 June, 2013 jointly organized by Dr.B.R.Ambedkar NIT, Jalandhar & CT Institute of Engg. Mgt. & Tech., Jalandhar.

- National Workshop on “Recent Advances in Microwave Circuit Design” from 18-19 August,2012 at Sachdeva Institute of Technology, Mathura under IEEE-MTTS Students Branch Chapter.
- Three-Day Hands on Program on “Analog System Design” during December ,2011 jointly conducted by TI University Program, Cranes and Thapar University at Thapar University, Patiala.

Personal Details:

- Adhaar No.: 977402793777 PAN No.: ANOPA4516G DoB: 02-07-86
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References:

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I hereby declare that information furnished above is true to the best of my knowledge.

Date: 04th October, 2025 **Dr. Prateek Agarwal**

Place: Haridwar (U.K.)